a camera signal processing circuit for receiving an output signal of said frame memory and performing a camera process.

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3. (Amended) The CCD imaging apparatus of claim 2, further comprising a first reproduced signal converter being capable of outputting a reproduced signal of said recorder unit at the first and second frame rates.

4. (Amended) The CCD imaging apparatus of claim 3, further comprising:

a viewfinder for displaying an output signal of said camera signal processing circuit; and

a second reproduced signal converter for converting the reproduced signal from said recorder unit to the second frame rate, and for outputting the converted signal to said viewfinder.

5. (Amended) The CCD imaging apparatus of claim 1,

wherein, when the first frame rate is below a specified number, said drive pulse switching circuit generates the CCD read pulse at the first frame rate, and generates the CCD drive pulse at the second frame rate, and

wherein, when the first frame rate is below the specified number, said frame memory stores the output signal of said CCD after the CCD read pulse, and reads out the stored output signal of said CCD n/2 times.

6. (Amended) The CCD imaging apparatus of claim 5, wherein the specified number is 30 frames/sec.

7. (Amended) The CCD imaging apparatus of claim 6, wherein the first frame rate is 24 frames/sec, 25 frames/sec, or 30 frames/sec, and n is 2.

8. (Amended) The CCD imaging apparatus of claim 1,

wherein said drive pulse switching circuit includes a frame rate equalizing controller for enabling said CCD to output both a signal of the first frame rate and a signal of a third frame rate at the second frame rate, the second frame rate being a common multiple of the first and third frame rates.

9. (Amended) The CCD imaging apparatus of claim 8, wherein the second frame rate is 60 frames/sec or 48 frames/sec.

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10. (Amended) The CCD imaging apparatus of claim 9, further comprising a recorder unit for recording a signal from said camera signal processing circuit at the first and third frame rates.

11. (Amended) The CCD imaging apparatus of claim 10, wherein said recorder unit reproduces a signal at the second frame rate.

12. (Amended) The CCD imaging apparatus of claim 10, further comprising a first reproduced signal converting circuit for issuing a reproduced signal of said recorder unit at the first and second frame rates.

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14. (Amended) The CCD imaging apparatus of claim 1,

wherein said CCD is of a multiple frame interline transfer (MFIT) type for reading out a progressive scanning signal divided into odd and even fields,

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wherein said frame memory outputs the signal in one frame in a segment frame (SF) format by dividing the signal into odd and even fields,

wherein said drive pulse switching circuit comprises a read field controller for generating a CCD drive pulse to control an order of the odd and even fields being output from said CCD, and for changing the order of the odd and even fields every one frame when n is an odd number at every frame.

15. (Amended) A charge coupled device (CCD) imaging apparatus comprising:

a CCD operable in a progressive scanning mode;

a drive pulse switching circuit for generating a CCD read pulse at a first frame rate, and for generating a CCD drive pulse at a second frame rate being n/2 times the first frame rate, n being an integer;

a CCD driver for driving said CCD;

a camera signal processing circuit for receiving an output signal of said CCD and performing a camera process;

a first frame memory for storing a first signal issued from said camera signal processing circuit in one frame after the CCD read pulse, and for reading out the stored first signal at a frame rate of the first signal n/2 times; and

a second frame memory for storing the first signal and reading out the stored first signal at the first frame rate, a reading out period of the first signal being n/2 frames.

16. (Amended) The CCD imaging apparatus of claim 15, wherein said second frame memory increases a number of samples in a horizontal blanking period of the first signal.

17. (Amended) The CCD imaging apparatus of claim 15, further comprising a recorder unit for recording and reproducing a signal issued from said second frame memory at a rate of the signal issued from said second frame memory.

19. (Amended) The CCD imaging apparatus of claim 15,

wherein, when the first frame rate is below a specified number, said

drive pulse switching circuit generates the CCD read pulse at the first frame rate, and generates the CCD drive pulse at the second frame rate,

wherein, when the first frame rate is below the specified number, said first frame memory stores the first signal, and reads out the stored first signal n/2 times, and

wherein, when the first frame rate is below the specified number, said second frame memory stores the first signal, and the read out period of the first signal is n/2 frames.

20. (Amended) The CCD imaging apparatus of claim 19, wherein the specified number is 30 frames/sec.

21. (Amended) The CCD imaging apparatus of claim 20, wherein the first frame rate is 24 frames/sec, 25 frames/sec, or 30 frames/sec, and n is 4.

22. (Amended) The CCD imaging apparatus of claim 15, further comprising a first reproduced signal converter being capable of issuing a reproduced signal of said recorder unit at the first and second frame rates.

23. (Amended) The CCD imaging apparatus of claim 22, further comprising a second reproduced signal converter for converting a reproduced signal of said recorder unit to the second frame rate, and

a switching circuit for issuing outputs of said first frame memory and said second reproduced signal converter.

24. (Amended) The CCD imaging apparatus of claim 15, further comprising a power on/off circuit for turning off said camera signal processing circuit while said camera signal processing circuit does not output the first signal

Respectfully Submitted,

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Enclosures: Version with Markings to Show Changes Made

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